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Ultrananocrystalline diamond-CMOS device integration route for high acuity retinal prostheses

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Abstract High density electrodes are a new frontier for biomedical implants. Increasing the density and the number of electrodes used for the stimulation of retinal ganglion cells is one possible strategy for enhancing the quality of vision experienced by patients using retinal prostheses. The present work presents an integration strategy for a diamond based, high density, stimulating electrode array with a purpose built application specific integrated circuit (ASIC). The strategy is centered on flip-chip bonding of indium bumps to create high count and density vertical interconnects between the stimulator ASIC and an array of diamond neural stimulating electrodes. The use of polydimethylsiloxane (PDMS) housing prevents cross-contamination of the biocompatible diamond electrode with non-biocompatible materials, such as indium, used in the microfabrication process. Micro-imprint lithography allowed edge-to-edge micro-scale pattering of the indium bumps on non-coplanar substrates that have a form factor that can conform to body organs and thus are ideally suited for biomedical applications. Furthermore, micro-imprint lithography ensures the compatibility of lithography with the silicon ASIC and aluminum contact pads. Although this work focuses on 256 stimulating diamond electrode arrays with a pitch of 150 μm, the use of indium bump bonding technology and vertical interconnects facilitates implants with tens of thousands electrodes with a pitch as low as 10 μm, thus ensuring validity of the strategy for future high acuity retinal prostheses, and bionic implants in general.

Keywords Microelectrode array · Microelectrode array-CMOS integration · High acuity retinal prostheses · 3-Dimensional microfabrication

1 Introduction

The evolution of retinal prostheses is intertwined with a class of implants with a large number of electrodes organised in a high density configuration. The aim of this approach is to develop a device with the potential to achieve both high acuity and high phosphene count, thus having a more significant benefit for recipients suffering diseases such as *retinitis pigmentosa*. Conventional ASIC silicon devices without a suitable biocompatible and hermetic coating are not a viable device beyond short term, acute implantation experiments (Hämmerle et al. 2002) due to their tendency to leach toxic elements as well as degradation of the device overtime. This raises the need for the encapsulation and packaging of the electronic devices with the stimulating electrodes located externally to the ASIC chip itself rather than using the chip's contact pads as stimulating electrodes. Many of the current retinal prostheses address this with an architecture based on planar interconnects between the stimulator electronics and

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the electrodes. In these devices, contact pads on the ASIC chip are connected to the stimulating electrodes using metallic planar "fan-out" tracks. Techniques such as multi-layer tracks (Guenther et al. 2011) or high resolution lithography (Guenther et al. 2012) exist for increasing the number and density of the fan-out tracks and ultimately increasing the number and density of stimulating electrodes. However the difficulty with these techniques is their lack of scalability whilst maintaining small pitch as the spacing between electrodes ultimately limits access for fan-out tracks. For instance, consider a typical case of planar tracks with a pitch size of 10 μm accessing electrodes with an interelectrode spacing of 100 μm and an electrode pitch size of 150 μm. In this configuration it is possible to access a row of 10 electrodes. In square electrode array configuration, this corresponds to twice of this, i.e., 20×20 electrodes over 3×3 mm area . As the technology for bionic implants further matures, it is likely that the electrode pitch will be reduced and the electrode count will increase. This makes the use of these planar approaches difficult for such implants.

The semiconductor industry has addressed the challenge of achieving packages with a high density and large electrode count through the use of vertical interconnects, as opposed to planar tracks. Flip-chip bonding is a widely used method to fabricate such interconnects. Flip-chip bonding involves patterning the contact pads of the ASIC chip with solder bumps which are bonded to the rest of the package using thermal, ultrasonic, or thermal-sonic approaches. Bond densities of 2500 per mm^2 (pitch size of 20 μm (Love et al. 2004)) are commonly used although 10,000~15,625 bonds per mm^2 (pitch=8~10 μm (John et al. 2004)) have been demonstrated. In comparison, a retinal prosthesis placed at an eccentricity of 2 mm from the fovea will target retinal ganglion cells with a density of approximately 16,000 cells per mm^2 (Curcio and Allen 1990). While the number of retinal ganglion cells is likely to be lower in target patents given the loss of cells which occurs in the diseased retina (Santos et al. 1997), a high density electrode array may still play a role in providing high acuity vision, particularly given the localised spatial variation in the ganglion cell density. Flip-chip bonding also opens the possibility for large number of independent stimulation electrodes, thanks to its high scalability in terms of total contact numbers. Indeed the forth mentioned works, which are adopted in here, report up to 4×10^6 electrical contacts.

The present work demonstrates a packaging strategy for retinal prostheses centred on the use of flip-chip bonding to achieve vertical interconnection between an ASIC chip and an all-diamond stimulating electrode array. It has been previously demonstrated that nitrogen doped ultrananocrystalline diamond (N-UNCD) exhibits key electrochemical attributes for its viable use as a microelectrode neuronal stimulator (Garrett et al. 2012; Hadjinicolaou et al. 2012). N-UNCD in conjunction with polycrystalline diamond (PCD), has been used to fabricate a hermetic electrical feedthrough array and subsequently an all diamond microelectrode array (Ganesan et al. 2014). The inherent properties of the diamond electrode array such as its mechanical reliability and strength (Ganesan et al. 2014), lightweight, thin form factor, biocompatibility (Bajaj et al. 2007; Tong et al. 2014), and biochemical stability (Zhou and Greenbaum 2010) make it ideal for use as a long lasting implant such as a retinal prosthesis. The construct of the diamond array lends itself for high density electrode integration and is easily scalable to higher numbers of electrodes and reduced pitch size (Ganesan et al. 2014) and therefore provides a means for achieving the high electrode density and count needed to provide high acuity vision through the elicitation of a large number of phosphenes. Furthermore, direct integration of the stimulating ASIC chip in the implant allows for a fully intraocular approach without puncturing the eye wall, and additionally provides the flexibility of utilising a wide range of stimulation strategies (Tran et al. 2014).

The approach presented here addresses the key requirements for the fabrication of bionic implants: 1) eliminate contact between exposed surfaces of the implant and potentially toxic materials such as indium which are present during the microfabrication process; 2) perform edge-to-edge microfabrication on components with small lateral dimensions; 3) perform microfabrication on non-planar samples; and 4) compatibility with hermetic sealing for encapsulation of an ASIC chip in a robust manner to ensure the extended life of the implant. The methods used herein in device packaging are based on mature industrial technology which benefits from ease of adoption in large scale manufacturing. This, combined with the use of scalable processes ultimately allows low cost integration of components for bionic devices.

Figure 1 illustrates the approach adopted in this work. A schematic cross-sectional view of a segment of the implant is shown in Fig. 1a. The implant consists of an ASIC which is flip-chip bump bonded using indium to conductive N-UNCD, used as diamond electrodes, which themselves are embedded in an insulating PCD, used as diamond matrix. The combination of flip-chip bump bonding and vertical diamond channels creates the possibility of creating a retinal implant with high pitch and electrode numbers. Figure 1b is micro-CT image of subsection of diamond based retinal prosthesis. The device consists of an array stimulating N-UNCD electrodes with a pitch of 150 μm flip-chip bump to an array of fan-out tracks. Although diamond is transparent in the microCT images, the metallic interconnects used within the device are evident in this figure.

2 Methods

An array of 16×16 diamond electrodes consisting of vertical channels of electrically conducting N-UNCD, embedded in

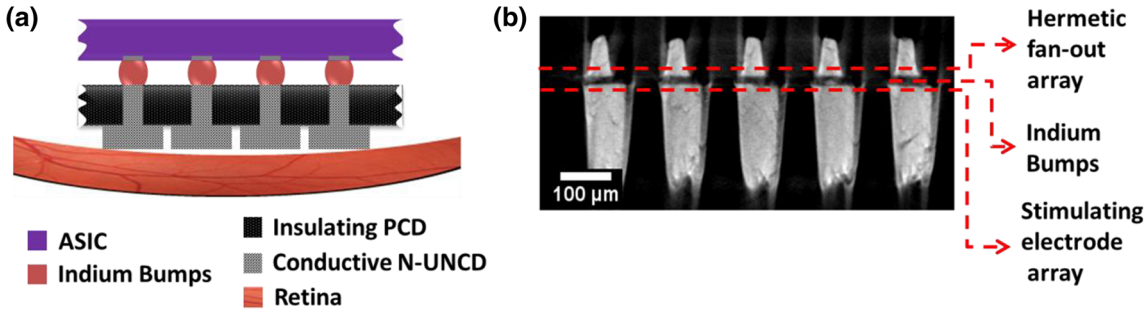

Fig. 1 **a** Schematic overview of a sub-section of high acuity retinal stimulator. The ASIC device is indium bump bonded to the stimulating N-UNCD diamond electrodes embedded in insulating PCD diamond. The vertical interconnects used in here facilitate a highly scalable device architecture for high count and density electrodes. The desire for minimum implant size for improved surgical outcomes, non-planar form factor that can conform to the retina's spherical shape, minimal cross-contamination on the surface of the diamond that is exposed to the body, and compatibility with hermetic packaging of the device undertaken in later stages of the fabrication process, require development of a number of technologies to address these challenges. The device integration strategy in this work facilitates edge-to-edge microfabrication on components with small lateral dimensions, eliminates direct contact between implant's external faces and toxic materials such as indium, allows microfabrication on non-planar samples, and is compatible with the steps necessary for with hermetic encapsulation of an ASIC device. **b** A micro-CT image of the implantable diamond based retinal prosthesis. The metallic interconnects, embedded in the diamond, show more strongly in the micro-CT image in contrast with the indium and diamond. Although this work demonstrates electrodes with a pitch size of 150 µm, the same technology is scalable to electrodes with smaller pitch sizes

insulating PCD were employed as electrode arrays. Figure 2a illustrates a cross sectional schematic of the diamond array. The electrical interface to the N-UNCD was enhanced through the use of a silver based active braze alloy (omitted in Fig. 2a). The total size of the diamond electrode array was 4×4 mm, with an electrode pitch of 150 µm. The fabrication process of the diamond electrode array has been reported previously (Ganesan et al. 2014).

The electrode array and ASIC, herein both referred to as the sample, are mounted separately onto a flat glass substrate with bonding pad side facing downwards using Crystalbond 905 ™ as shown in Fig. 2b. This approach ensured that the sample was mechanically secured and avoided leakage of polydimethylsiloxane (PDMS, Sylgard 184) onto the contact pads in the subsequent step. The PDMS, mixed with the ratio of 1:10 hardener to elastomer, was degased under vacuum and

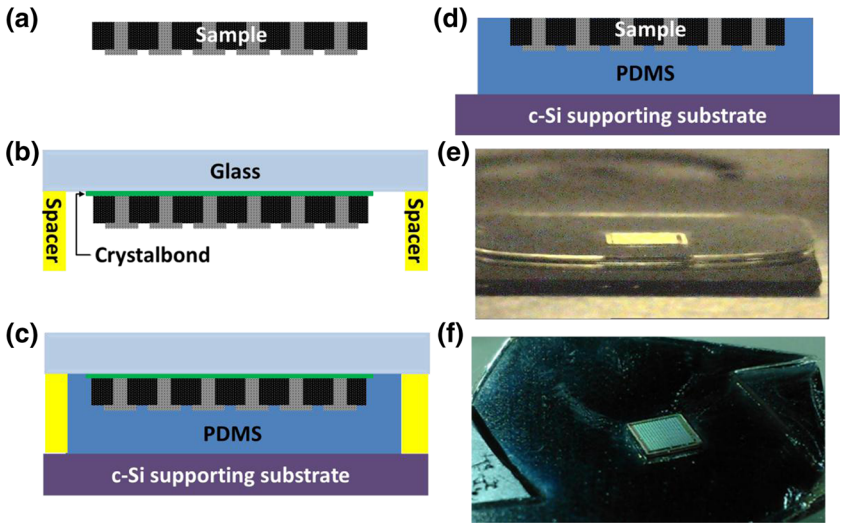

Fig. 2 Fabrication of the work piece incorporating both the PDMS housing and the sample. **a** The initial sample, in this instance an electrode array, with the contact pads facing upwards. *Light grey* indicates the conductive N-UNCD channels within the insulating PCD (black). **b** Sample and two spacers are mechanically secured to a glass substrate (*light blue*) using crystalbond (*green*) with the contact pads facing the glass substrate. **c** PDMS (*dark blue*) is poured over the sample and a silicon supporting substrate (*purple*) is placed firmly at the back of the sample. **d** The glass substrate and spacers are removed creating the work piece consisting of silicon supporting structure, PDMS housing and the sample itself. The use of the spacers ensures that the silicon supporting substrate and the surface of the sample is parallel, thus providing a suitable work piece for microfabrication, even if the sample itself does not meet this form factor requirement. **e** side, and **f** top view microscope images of work pieces incorporating an ASIC device within the PDMS housing. The same approach is used for moulding of both the diamond electrode array and ASIC device. The schematics are not drawn to scale

poured over the sample to cover its back and sides as shown in Fig. 2c. A separate crystalline silicon substrate was joined firmly on the back of each sample to provide mechanical stabilisation and support during the fabrication process. The PDMS was then cured at 60 °C in a desiccator and the glass substrate removed to expose the bonding pads on the samples as illustrated in Fig. 2d. Crystalbond residues are dissolvable in acetone and were removed by solvent cleaning involving ultrasonication of the sample in acetone followed by isopropanol and then rinsed in deionised water.

Following PDMS moulding, solvent cleaning, oxygen plasma cleaning (20 min) and de-hydrogenation bake (180 °C, 30 min), the work piece incorporating both the sample and its PDMS housing, was spin coated (3000 rpm) with a thin film of poly methyl methacrylate (PMMA 950 A8) dissolved in anisole, and softbaked at 180 °C for 300 s. The work piece was subsequently coated with AZ4620 positive tone photoresist (Microchemicals Inc.) at 2000 rpm for 3 s, followed by 500 rpm for 300 s and softbaked at 105 °C for 60s resulting in 30 μm thick resist films. Micro-imprint lithography was used to pattern the PMMA/AZ4620 bilayer. The stamp consisted of laser micro-machined chemical vapour deposited (CVD) 500 μm thick PCD as illustrated in Fig. 3a and b. The sidewalls connecting the vertical pillars are an artefact of the stamp fabrication process. Micro-imprinting was performed at 105 °C over a period of 60s, with a force of 10 N (3.75cN per 40×40 μm pillar or 23.4 N/mm^2). A discussion on the choices of the resist is provided in Section 3.1.

Following the micro-imprinting patterning step, the work piece was placed in 20/80 % oxygen/argon plasma to remove the final residues of the resist. Under-bump metallisation (UBM) consisting of a 50/50/20 nm Ti/Ni/Au e-beam evaporated tri-layer was deposited on the diamond array. In the case of the ASIC chip, the formation of an insulating aluminium oxide layer on the aluminium contact pads necessitated *in situ* dry argon plasma etching prior to the evaporation of the UBM. (The aluminium oxide formation is a side effect of the fabrication process and storage and therefore it needs to be addressed in order to achieve consistent bump electrical performance). The Argon plasma etch conditions wereoptimised to remove a 5 nm thick layer of aluminium oxide prior to the UBM evaporation of 50/50 nm Ti/Pt bilayer.

Following UBM evaporation, and without removing the patterned photoresist, both the diamond electrode array and the ASIC chip were coated with a 10 μm indium film. The evaporation was performed thermally at a rate of 5 Å/s over several hours. Given the long duration of the evaporation and the low melting point of indium, it proved necessary to perform the evaporation in a specially adapted thermal evaporator (PVD-75, Kurt J. Lesker inc.) with a water cooled stage in order to avoid indium reflow due to overheating of the sample during evaporation. Following evaporation, the work pieces were placed in an acetone bath at room temperature to dissolve the PMMA-photoresist bilayer for the lift-off step. This was followed by solvent cleaning, de-ionised water rinse, and oxygen plasma surface cleaning. Figure 4 summarises the steps used for patterning the indium bumps.

Flip-chip bonding was performed at a maximum stage temperature of 170 °C for 30s using a force of 25 N in a formic acid atmosphere to remove any indium oxide formed. Both prior to, and after the flip-chip bonding step, the samples underwent a reflow step at a maximum temperature of 200 °C for 60s in a formic acid atmosphere to improve the bump adhesion, and allow the sample to self-align to address any marginal misalignment. Following flip-chip bonding, underfill epoxy was applied to the gap between the chip and diamond array using capillary force. The epoxy resin EpoFix (Struers) was chosen due to its low temperature curing of 30~40 °C, low viscosity of 550 cP, and excellent adhesion to diamond and silicon.

DC electrical characterisation of the final, flip-chip bonded device was performed in a probe station using a 6487 picoammeter/voltage source (Keithley Instruments). The electrical resistance of the bumps were characterised by

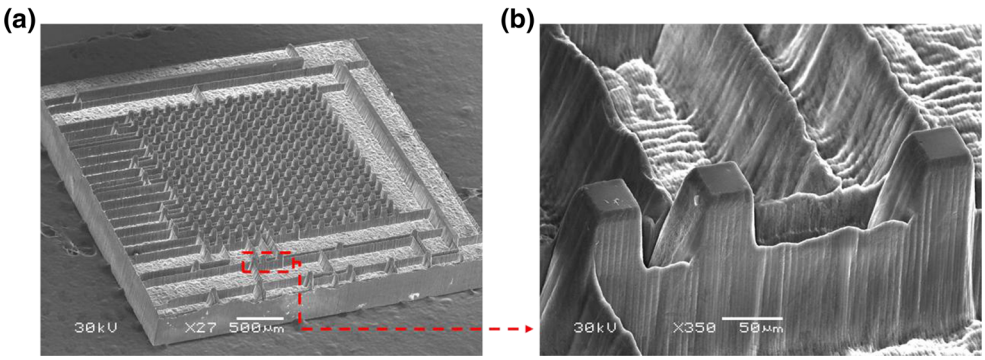

Fig. 3 **a** Diamond micro-imprint lithography stamp used for patterning the diamond array. A second diamond stamp (not shown here) with complementary mirrored pattern was used for the ASIC device. The stamp is created by laser micro machining a 500 μm thick PCD. It contains 256 pillars with a pitch of 150 μm for patterning the electrode array, in addition to pillars for patterning interface contacts such as power and data as illustrated in **b**. The minimum pitch size here is 100 μm

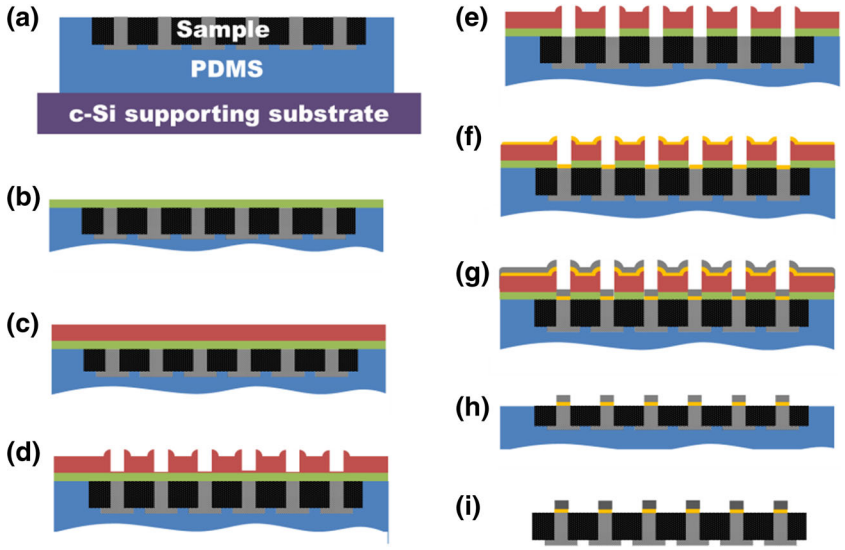

Fig. 4 The indium bump patterning process: **a** Schematic of a work piece incorporating an electrode array. **b** The work piece is spin coated with a 50 nm thick PMMA resist (*green*) and softbaked. **c** A 30 μm layer of AZ4620 photoresist (*red*) is spin coated on top of the PMMA and softbaked. **d** Mico-imprint patterned PMMA/AZ4620 photoresist layers with a thin layer of residual resist remaining. **e** Oxygen plasma is used to remove resist residues thus fully opening the patterns. **f** UBM evaporation (*yellow*). This consists of 50/50/20 nm Ti/Ni/Au for the diamond electrode array and Ar plasma *in situ* etch followed by 50/50 nm Ti/Pt for the ASIC. **g** Following the UBM evaporation a 10 μm thick layer of indium (dark gray) is thermally evaporated. **h** The work piece is soaked in acetone at room temperature to lift off the resist and expose the patterned indium and UBM. **i** Sample with the patterned indium bumps is removed from the work piece

fabricating a daisy chain type sample outlined in the electrical characterisation section of this paper. An electrochemical impedance spectrum of each stimulating electrode was measured against a platinum counter electrode using the Z100 electrochemical impedance analyzer (eDAQ Pty Ltd) with saline salt bridge.

3 Results & discussion

3.1 Fabrication considerations

Embedding the sample in a PDMS housing offers a number of advantages when working on bionic microdevices. By extending the flat surface of the sample so that the edges of the plateau are far from the region of interest, the PDMS housing results in a significantly more uniform thickness of spin coated resist across the sample by shifting the edge beads away from the sample edge to the edge of the PDMS housing. The absence of edge beads on the samples edges opens up the possibility of edge-to-edge patterning, thus allowing the development of implantable devices with minimal dimensions with the aim of improved surgical outcome. For example the ASIC device used in this work has a dimension of 2.9×3.15 mm with electrodes located at 100 μm from the edge of the chip. Furthermore, the PDMS housing acts as a protective barrier against the exposure of the exterior facets of the implant to toxic materials (e.g., indium and photoresist) used during microfabrication steps, thus preventing the risk of cross-contamination – a key consideration in fabrication of bionic devices. Within the housing, the diamond electrodes which will ultimately come in contact with the neural tissues are protected throughout the fabrication steps. Moreover this approach creates space for handling the work piece, eliminating the need for direct handling of the sample itself during microfabrication, thus eliminating the risk of damage to samples by handling. This is particularly important given the presence of key electrodes at the edge of the sample, where direct handling of the sample with tweezers risks damage to its features.

A key feature of the PDMS housing developed is the parallelism between the silicon supporting substrate and the surface of the sample, achieved through the use of spacers as illustrated in Fig. 2. The spacers used here consist of 500 μm thick c-Si wafer fragments. Many bionic implants are structured to conform to the shape of various body organs with the aim of enhancing the mechanical and electrical interaction between the implant and body. This particularly important for high acuity retinal prostheses which require a very small gap between the stimulating electrodes and the retina (Opie et al. 2014). Methods such as laser micro-machining are commonly used to create implants with curvatures that closely match the intended organ, such as the retina (Opie et al. 2014) . The use of PDMS housing in this work creates a temporary work piece with a key feature that the top and bottom surfaces are parallel to each other, even if the sample itself is non-parallel. This feature allows the use of conventional microfabrication techniques on the sample embedded in the

work piece, which would otherwise be impossible for a non-parallel sample.

A bilayer of AZ6420 and PMMA was necessary in this work to prevent distortion of the lithographic pattern. The AZ4620 photoresist is selected as the micro-imprint lithography resist. Propylene glycol monomethyl ether acetate (PGMEA) is the main solvent in this type of resist. This solvent is highly absorbable by PDMS (up to 27 wt.%) (Kim et al. 2001) which results in penetration and retention of the resist's PGMEA solvent within the PDMS housing. This significantly distorts the photoresist's softbake time and temperature profile which can potentially be addressed in the case of thin resists. However in the case of the thick photoresist (30 μm) used for lift-off of indium film, which in this work has a thickness of 10 μm, the presence of PGMEA reservoirs in the PDMS leads to unreliability of the softbaked resist. A typical challenge encountered in using thick photoresists on conventional substrates is surface hardening of the resist during the softbake step. Since this invariably occurs prior to sufficient solvent evaporation across the bulk of the resist, solvents are thus trapped in the bulk of the resist. Although this challenge can be addressed through adjustment of the softback temperature and duration profile, this approach proved to be ineffective in this work due to the presence of a significant reservoir of PGMEA within the PDMS. The gradual back diffusion of the PGMEA from PDMS into the resist results in the severe unreliability of photoresist due to the poor resist properties following softbake. A typical indicator of this effect was the formation of bubbles, also known as foaming, on the surface of the softbaked resist during high vacuum processes, particularly when substrate thermal heating is present (e.g., oxygen plasma cleaning or metal evaporation). Here, the combination of low pressure and sample heating leads to the evaporation of the remaining PGMEA solvent from the sample. These vapours are partially blocked due to the presence of a relatively hardened crust at the surface of the photoresist, thus leading to the formation of bubbles on the surface of the photoresist. Although these bubbles appear on the PDMS and not the sample itself, they result in the distortion of resist patterns close to the PDMS-sample interface and subsequent unreliability of features at the sample edge. The goal of edge-to-edge sample patterning is achieved by developing a reliable thick resist on the PDMS housed sample through the use of a thin barrier layer to minimise the interaction between resist and PDMS. PMMA dissolved in anisole was selected for this purpose. Anisole exhibits negligible absorption in PDMS (Du Plessis et al. 2002), whilst fully baked PMMA does not interact with photoresist. Therefore, using PMMA as a barrier layer between the PDMS and photoresist effectively decouples the interaction between the two layers, therefore leading to a better quality coated photoresist.

A key advantage of micro-imprint lithography is that it eliminates the need to use photolithographic developers, many of which are incompatible with aluminium terminated contact pads on the ASIC. The majority of developers, both those incorporating metal ions and those metal ion free, are not compatible with either aluminium or silicon due to the selective etching of these materials and subsequently have the potential for severe ASIC degradation. The micro-imprint lithography used in this work is a developer free process thus making it fully compatible with the ASIC chip.

The mechanical robustness of the diamond imprint stamp means micro-imprint lithography can be used to create highly reproducible patterns over multiple micro-imprinting steps. Moreover diamond's rigidity makes it possible to fabricate stamp features with very high aspect ratios, otherwise not possible with conventional micro-imprint lithography stamps based on flexible materials such as PDMS. Finally the inherent chemical inertness of diamond is compatible with aggressive cleaning techniques, such as piranha cleaning, which results in minimal sample contamination without any degradation of the features or the lifetime of the stamp. However, unlike its elastic counterparts, such as PDMS stamps, the rigidity of the diamond mandates a high degree of co-planarity between the stamp and the sample to ensure uniformity of pattern transfer across the entire sample. The flip-chip bonder is an ideal tool for performing this task as it is designed for the attachment of two work pieces in a co-planar fashion. The bonder is adjusted to facilitate the placement of stamp on the sample in a manner that the vertical gap between the surface of the stamp features and the sample surface is constant throughout the lateral dimensions thus ensuring that the photoresist is patterned uniformly over the entire surface of the sample.

The indium bump bonding force used here corresponds to ~9.4cN/bump which is significantly higher than the force used in other works on indium bump bonding (~1cN/bump) (Das et al. 2009). The comparatively large force used here proved necessary due to the relatively large dimensions of the indium bumps used in this work. For example the indium bumps used in this work have lateral dimensions of 50×50 μm which corresponds to approximately 10 times the area of an indium bump with lateral dimension of 15×15 μm (Das et al. 2009), and correspondingly requires ~10 times larger force. Prior to the application of the force, gaseous formic acid was introduced in the bonding chamber to remove the native oxide residue from the surface of the indium bumps and the sample was heated up to the maximum temperature of 220 °C. It has been demonstrated that the formic acid atmosphere is most effective at removal of the oxide layer from indium at temperatures above 200 °C (Lin and Lee 1999).

3.2 Micro-imprint patterning

The PDMS housing allows uniform coating of resist over the critical area of the sample proper. Fig. 5a), is an optical profile image of the patterned photoresist on the diamond electrode

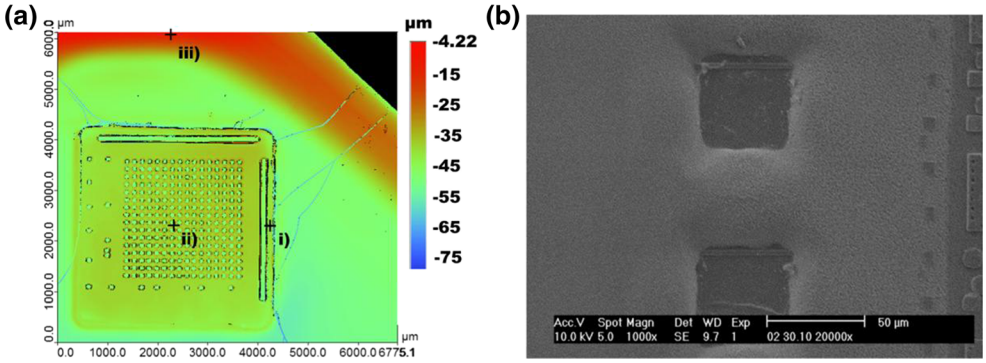

Fig. 5 **a** An optical profilometer image of spin coated and patterned photoresist on a work piece consisting of diamond electrode array embedded in PDMS housing. The height difference between points iii and ii, located at the edge of the work piece and centre of the diamond array respectively, is 36 µm corresponding to 120 % difference in the thickness of the resist due to the edge bead formation. Such a large thickness variation in undesirable in microfabrication processes. The height difference between the points ii and i, located at the centre of the diamond array and the edge of the diamond array, is 3.3 µm corresponding 11 % difference in the thickness of the resist and therefore making the edge to edge patterning of the sample possible. **b** SEM image of patterned resist on two contact pads on the ASIC device. The contact pads with the spacing of 30 µm are located 150 µm from the edge of the ASIC device

array. The sample is embedded in a PDMS housing such that the surfaces of the sample, electrode array in Fig. 5a, and the PDMS housing are seamlessly flush. The absence of pronounced step height features at the sample/PDMS housing interface allows spin coating of resist of a uniform thickness. The PDMS serves to extend the edge of the work piece away from the actual sample's edge. This prevents the phenomenon of edge beading that occurs at the edges of spin coated samples due to surface tension of the photoresist. Here the edge bead is removed from the edge of the sample (location i. in Fig. 5a) to the edge of the PDMS work piece (location iii. in Fig. 5a). The 3.3 µm thickness difference between the centre and the edge of the sample, locations ii. and i. respectively, corresponds to 11 % of the 30 µm resist thickness. This is a significant improvement over the 36 µm height difference between the centre of the sample and the edge of the work piece, locations ii. and iii., which corresponds to 120 % of the total resist thickness.

As demonstrated in Fig. 5a the PDMS housing allows spin coating a uniform and thick layer photoresist for edge-to-edge patterning using imprint lithography. Figure 5b shows an SEM image of patterning resist on the ASIC device. The openings in the resist films are over contact pads with a spacing of 30 µm, located at 150 µm from the edge of the ASIC device. As illustrated by this image, the use of PDMS housing, in conjunction with imprint pattering, makes patterning of such structures a viable possibility.

Micro-imprint lithography offers a number of advantages over conventional lithography which are critical to the fabrication of bionic devices. Unlike photolithography which requires direct and continues contact between the photomask and photoresist, micro-imprint lithography does not require such contact. The contacts are instead made through penetrating pillars. This makes the process adaptable for use in patterning of non-planar samples with a wide range of form factors. This may include samples which lack co-planarity between the front and back of the sample as well as samples with patterns that are non-polarised on the surface with features which are recessed relative to the surface of the sample This flexibility allows for a range of high-temperature techniques such as laser micromachining and brazing to be used to shape various components of the implant, in a non-planar fashion prior to integration step. Given the high temperature nature of these processes, they typically cannot be performed following the device integration. For example, Fig. 6a shows a side view image of a diamond-based retinal stimulator fabricated using the technology outlined in this work. The implant consists of a diamond stimulating electrode array and a diamond plate with an array of platinum wire feedthroughs brazed in place, both with internal metallic tracks. The metallic pads on both diamond plates are electrically bonded using indium bumps. As illustrated, the components used for the fabrication of the implant are not flat at the component level: the brazed platinum wire feedthrough array used as external interconnects located on the back side of the implant and the laser micro-machined electrode array at the front of the samples result in a non-planar sample for lithography.. Despite this, micro-imprint lithography provides a suitable platform for patterning indium bumps on the internal contact pads of the implant's individual components. An optical profilometer image in Fig. 6b shows these indium bumps precisely and uniformly patterned on the sample using the imprint lithography technique. The integration method outlined in this work provides a sufficient degree of control for the patterned bumps on the two diamond samples to be aligned and bump bonded to each other as depicted by the microCT image of the implant Fig. 6c. Here, the three dimensional illustration of metallic tracks embedded within the diamond implant and the indium bump bonded vertical interconnects for direct access to the stimulating diamond electrodes are illustrated. The interface

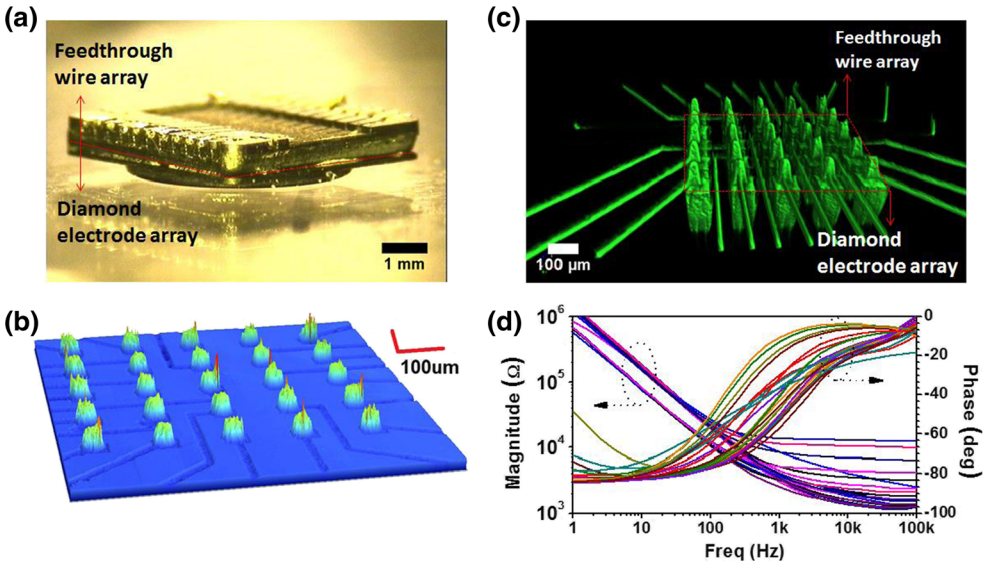

Fig. 6 Micro-imprint lithography of three dimensional diamond structures used for fabrication of diamond based retinal stimulating array. **a** Side view of an implantable device consisting of two components; laser micro-machined diamond array at the bottom half and platinum wire feedthrough array for external implant connection at the top half. The image highlights the non-planar nature of the sample. **b** Optical profilometer image of patterned indium bumps using micro-imprint lithography on metallic tracks embedded within the diamond sample. A sufficient degree of alignment, better than 10 µm, and reproducibility can be achieved. **c** A microCT scan yielding a three dimensional reconstruction of the implantable device showing the degree of alignment for bump bonding of the two halves of the sample achieved in order to demonstrate vertical interconnects for high density and count stimulating electrode array. **d** Electrochemical impedance measurement on the electrodes of implant used for retinal stimulation measured in buffered saline solution. Arrows are indicator of the appropriate axis. The average impedance at 1 kHz is 4.8kΩ with standard deviation of 2.7kΩ. The phase at 1 kHz is in the range of −60 to −100°, which as expected indicates a capacitive behaviour

between the two diamond samples is highlighted, showing a sufficient degree of alignment for the 150 µm pitch vertical interconnects using flip-chip bonded indium bumps. This implantable test structure contained an array of 5×5 stimulating electrodes. The platinum wires at the back of the implant facilitated direct access to each of the electrodes.

The electrochemical impedance spectra of the 25 diamond electrodes measured in buffered saline solution are shown in Fig. 6d, with an average impedance of 4.8kΩ at 1 kHz and a standard deviation of 2.7kΩ. The diamond electrodes prior to undergoing the integration process exhibited an impedance of 2.3 kΩ and standard deviation of 0.16 kΩ. The higher electrochemical impedance and standard deviation can be attributed to the contamination of the diamond surface with the PDMS. Based on the impedance measurement, constant-current pulses with a magnitude of 200 µA can be used for retinal stimulation whilst limiting the stimulation voltage to below 1 V safe limit (Ganesan et al. 2014) thus avoiding potential cell damage due to the electrolysis of water. This results in a maximum charge injection capacity of 2×10^{-8}C when stimulating with a 100 µs current pulse. For our 120 μm^2 electrodes, this corresponds to a charge injection density of 0.14 mC/cm^2, which greatly exceeds the charge injection density of 0.050+/−0.005 mC/cm^2 that has been demonstrated for achieving high resolution stimulation of ganglion cells using epiretinal stimulation (Sekirnjak et al. 2008). Overall, the low electrochemical impedances shown here demonstrates the feasibility of using vertical interconnects for addressing individual diamond electrodes configured as a high density and high electrode count stimulating array.

3.3 Electrical properties

Electrical performance of the bumps was examined by measuring their DC resistance. This was performed by fabricating a "daisy-chain" type test structure, consisting of metallic tracks with complementary segments on two samples which, when bump-bonded to each other to form a continuous chain through the bumps, as shown in Fig. 7a. The contribution of each track segment and bump to the total chain resistance can be extracted from the slope of a plot of resistance of chains with increasing numbers of segments. The test consisted of 16 chains. Each chain contained 16 bumps with a diameter of 50 µm, yielding a total of 256 bumps. The metallic tracks joining the bumps were 150 µm×75 µm in size, separated by 100 µm, and had the same composition as the UBM used in the vertical interconnects in the integration process (20 nm/50 nm/50 nm of Ti/Ni/Au). The resistance as a function of the number of bumps is presented in Fig. 7b, with slope of 770 mΩ per segment (bump and track) in the linear region. One possible reason for this nonlinearity is that non-uniformities in the evaporated track thickness could have a dominant effect; uncommon in short tracks but likely in long tracks. This is further evident in Fig. 7b, where the significant

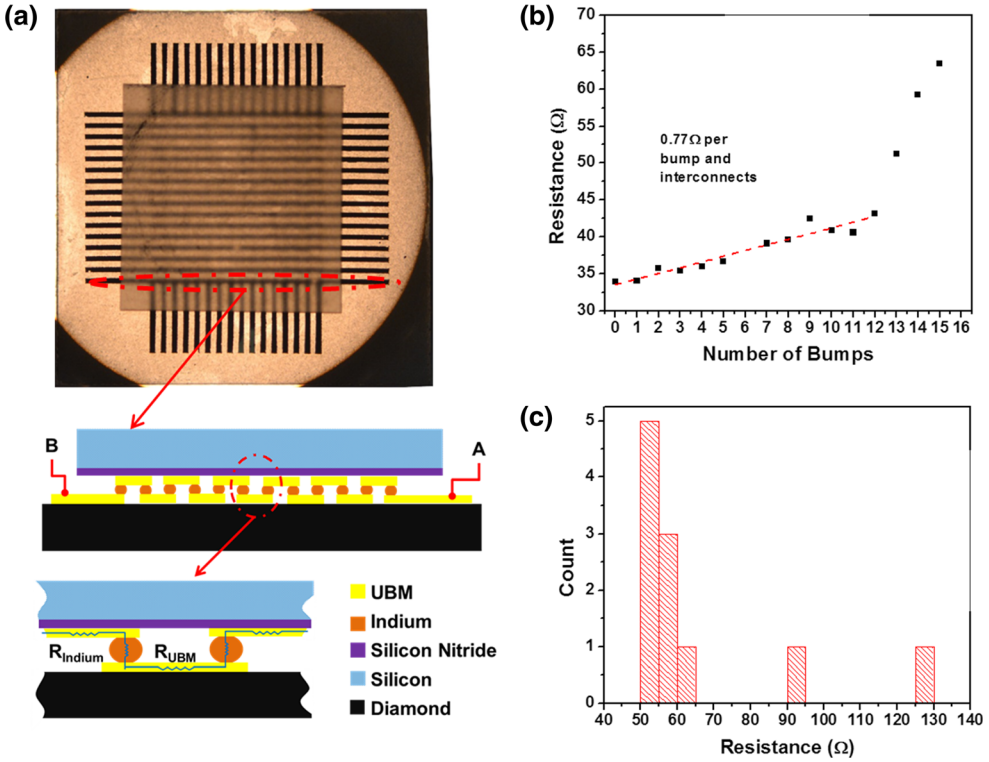

Fig. 7 **a** Top view microscope image and cross sectional diagram of test structure used for the electrical characterisation of the indium bump vertical interconnect. The structure contains 16 daisy chains each with 16 indium bumps joined by metallic track segments. **b** Resistance measured as a function of number of bumps in a daisy chain. The resistance of one segment (bump and track of interconnect) is 770mΩ, extracted from the linear region. The observed nonlinearity at higher bump numbers are attributed to non-uniformities in the thickness of interconnects and are omitted from the bump resistance calculations. **c** Histogram of impedance resistance of daisy chains illustrating 50 % of the chains have a resistance below 60Ω. This value, which includes both indium bumps and interconnects resistance, is dominated by the interconnect resistance

non-linearity observed at higher number of indium bumps could be due to non-uniform deposition of the metallic tracks across the sample. The increase in the resistance of the daisy chains due to the tracks' non-uniformity affected only 3 of the chains, which was determined by the fact that the chain total resistance was above 60Ω, as illustrated in Fig. 7c. Based on this, the non-linear portion of Fig. 6b was disregarded during bump resistance calculations. A calculated estimated value of track resistance based on its geometry is 765 mΩ. Alternatively, the track resistance was extracted using two point current–voltage measurement of a 1900 μm continuous track with a value of 33.9Ω. Based on this approach, the resultant track resistance between each pair of bump is 1.5Ω. Although using either of these approaches the true value of bump resistance could not be determined, it is evident that the track impedance has a dominating effect, with the true bump resistance below that of 770 mΩ.

Overall, the variability of the bump impedance was examined by measuring all of the daisy chains within the test structure as presented in Fig. 7c. Using this process, 93 to 99 % continues bump yield was attainable.

Low electrical resistances of the interconnects are important for the correct operation of the ASIC device. A typical electrical stimulus for neural stimulation takes the form of a train of biphasic current pulses. However, the excitability of a neuron is often reported in terms of charge and charge density, as excessive amounts of absolute charge and charge density may result in electrode and/or tissue damage. Low impedance for neural stimulating electrodes is desirable to ensure the delivery of sufficient current to excite neural cells within safety limits, as well as within the compliance voltage of the ASIC chip. Therefore, it is imperative that the contribution to the electrode impedance of the indium bumps is minimal. Any significant resistance of the electrode interconnects, including indium bumps, relative to the electrochemical impedance of the electrodes would limit the ASIC chips current delivery with its compliance limits (~3 V used in this work in order to minimise the power consumption and geometric footprint of the ASIC device). This leads to a limited current density and subsequently the charge available for neural stimulation. Moreover considering the electrochemical stimulating electrodes as a capacitive elements and interconnects, including indium bumps, as a resistive elements will lead to a characteristic time constant of the circuit which may distort the stimulation waveform. From the device safety point of view low resistance interconnects, including indium bumps, play an

imperative role. Achieving the condition where resistance of interconnects is significantly lower than the electrochemical impedance of the electrodes fulfilled the assumption that the stimulation voltage waveform delivered by the ASIC device is approximately identical to the voltage at electrode-solution interface. This is because of minimal voltage drop across the interconnects. Using this assumption it is possible to design an implant where the stimulating electrode voltage is accurately capped below the electrochemical water window of the electrode thus preventing the possibility of long term electrode or tissue damage due to the water splinting. Finally low impedance interconnect ensures reliability of power/data transmission on the implanted chip.

3.4 Thermal performance

A commonly encountered phenomenon in flip-chip bonded devices is thermally activated failure, which is typically caused by significant mismatch in thermal expansion of the components in the assembly. When exposed to repeated thermal cycles, this mismatch results in repeated mechanical stress in the bumps and subsequently mechanical failure due to cracks through the bumps or delamination. These fatigue failures are minimised through the use of underfill epoxy, which strengthens the bump bonds.

In this work, the assembly consisted of a silicon based ASIC bump bonded to a PCD-based diamond array. The thermal expansion coefficient of crystalline silicon (2.3 ppm/K) closely matches that of the CVD grown PCD (1.21 ppm/K) compared with organic FR4 substrates (18–24 ppm/K) (Zhang and Wong 2004). This makes the device inherently resistant to the effects of thermal cycling. Furthermore, unlike consumer electronics, bionic implants typically experience a near constant thermal profile throughout operation in the human body, thus limiting the total number of thermal cycles experienced by the implant. Despite this fact, the high degree of mechanical stability that is conferred mandates the use of underfill epoxy. To examine the effect of thermal cycling on the implant, a single daisy chain test structure was subjected to 100 thermal cycles from 40 to 100 °C. Following thermal cycling, no observable change was found in resistance. The small number of thermal cycles and temperature range selected here reflect the upper limit of thermal cycling an implant might encounter.

In addition to thermal cycling, the underfill epoxy is required to withstand a number of thermally driven processes, most critical of which is sterilisation. Dry and wet heat sterilisation are commonly used methods in the preparation of implantable devices (Laroussi and Leipold 2004). Fig. 8 shows the effect of heating on the flip-chip bonded daisy chain assembly. The duration of heating was 10 min. When heated to temperatures up to 250 °C, the flip-chip bonded device remained stable. This was confirmed by the absence of change in resistance of the daisy chains. Despite the fact that above 156 °C the indium bumps are in a molten state, the mechanical stability of the underfill epoxy between the diamond and

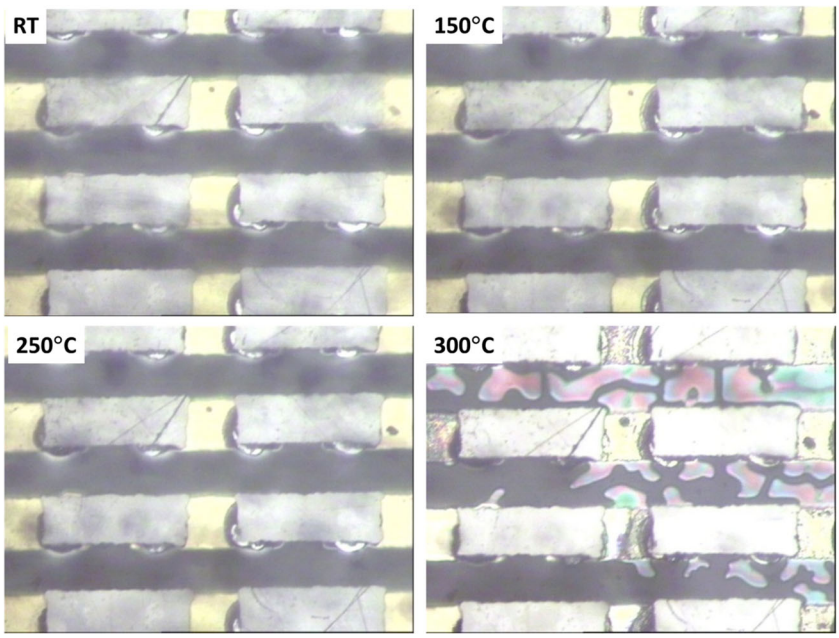

Fig. 8 Optical microscope image of a heated flip-chip bonded device consisting of optically transparent diamond, underfill epoxy and silicon chip. The metallic tracks are portion of a daisy chain test structure. No change in the room temperature chain resistance was observed following heated treatment of the sample below indium's melting point (150 °C) for 10 min. Above indium's melting point, there was also no change in the chain's room temperature resistance when the sample was heated up to 250 °C for 10 min. However beyond 280 °C open circuit connections started to appear and at 300 °C all the daisy chains where open circuited. The change in the colour observed at 300 °C is due to epoxy swelling and subsequent delamination which is accompanied by disconnected indium bumps, releasing molten indium

silicon was sufficient to maintain electrical integrity. As the temperature is raised above 280 °C, an abrupt failure in the bumps was observed. The failure mode was open-circuit and can be attributed to the swelling of the epoxy, as the epoxy's coefficient of thermal expansion increases sharply above its glass transition temperature. This is clearly illustrated by the appearance of thin film interference colours in Fig. 8 at 300 °C due to the delamination of epoxy from the diamond.

4 Conclusion

This work outlines a strategy to integrate an electrode array with a high count and high density of electrodes with a stimulator ASIC. The strategy was demonstrated using an all-diamond, 256-channel stimulating electrode array and a custom-built ASIC device designed to safely stimulate retinal tissue for restoring vision. Flip-chip bonding of indium bumps was used to create high-count and high-density vertical interconnects. The innovation of a PDMS housing allowed edge-to-edge patterning of non-planar substrates, for example those that are designed for biomedical applications and conform to the shapes of body organs. The PDMS housing also prevented cross-contamination of the biocompatible electrode array with toxic materials used during microfabrication. Micro-imprint lithography eliminated the need for corrosive developers, ensuring compatibility of this lithographic technique with the silicon ASIC and aluminum contact pads.

Electrical and electrochemical performance of the bump bonded test assembly was examined. The combined bump and track resistance was 770mΩ, which can be considered as an upper value of the bump resistance. This value, dominated by the track resistance, is small enough to facilitate optimal operation of the ASIC device, and contributes negligibly to the electrode's electrochemical impedance. Once the array was integrated with the ASIC, the electrodes exhibited an electrochemical impedance of 4.8KΩ, which is well within the required range for use as stimulating electrodes (Green et al. 2008) and far below the bump resistance demonstrated in this work.

Although this work is demonstrated using 256 stimulating diamond electrode arrays with a pitch of 150 μm, this combination of indium bump bonding technology and vertical interconnects facilitates implants with high number of electrodes, tens of thousands and beyond, with pitch as low as 10 μm ensuring validity of the strategy for future high acuity retinal prostheses.

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